

# NDF04N62Z, NDD04N62Z

## N-Channel Power MOSFET 620 V, 2.0 Ω

### Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode-Protected Gate
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Parameter	Symbol	NDF	NDD	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	620		V
Continuous Drain Current R <sub>θJC</sub>	I <sub>D</sub>	4.4 (Note 2)	4.1	A
Continuous Drain Current R <sub>θJC</sub> , T <sub>A</sub> = 100°C	I <sub>D</sub>	2.8 (Note 2)	2.6	A
Pulsed Drain Current, V <sub>GS</sub> @ 10V	I <sub>DM</sub>	18 (Note 2)	16	A
Power Dissipation R <sub>θJC</sub> (Note 1)	P <sub>D</sub>	28	83	W
Gate-to-Source Voltage	V <sub>GS</sub>	±30		V
Single Pulse Avalanche Energy, I <sub>D</sub> = 4.0 A	E <sub>AS</sub>	120		mJ
ESD (HBM) (JESD22-A114)	V <sub>esd</sub>	3000		V
RMS Isolation Voltage (t = 0.3 sec., R.H. ≤ 30%, T <sub>A</sub> = 25°C) (Figure 14)	V <sub>ISO</sub>	4500	-	V
Peak Diode Recovery	dv/dt	4.5 (Note 3)		V/ns
Continuous Source Current (Body Diode)	I <sub>S</sub>	4.0		A
Maximum Temperature for Soldering Leads, 0.063" (1.6 mm) from Case for 10 s Package Body for 10 s	T <sub>L</sub> T <sub>PKG</sub>	300 260		°C
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Limited by maximum junction temperature
3. I<sub>SD</sub> = 4.0 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, T<sub>J</sub> = +150°C

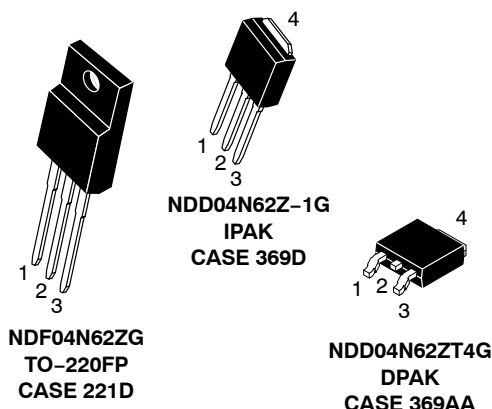
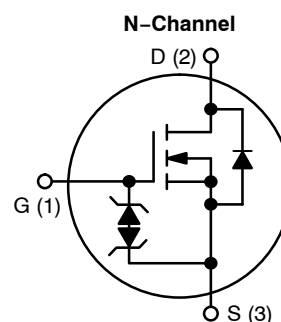
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V <sub>DSS</sub>	R <sub>DS(ON)</sub> (MAX) @ 2 A
620 V	2.0 Ω



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# NDF04N62Z, NDD04N62Z

## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	NDF04N62Z	4.4	°C/W
	NDD04N62Z	1.5	
Junction-to-Ambient Steady State	(Note 4) NDF04N62Z	50	
	(Note 1) NDD04N62Z	38	
	(Note 4) NDD04N62Z-1	80	

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	BV <sub>DSS</sub>	620			V
Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> = 1 mA	ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>		0.6		V/°C
Drain-to-Source Leakage Current	V <sub>DS</sub> = 620 V, V <sub>GS</sub> = 0 V	I <sub>DSS</sub>	25°C		1	μA
			125°C		50	
Gate-to-Source Forward Leakage	V <sub>GS</sub> = ±20 V	I <sub>GSS</sub>			±10	μA

### ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.0 A	R <sub>DS(on)</sub>		1.8	2.0	Ω
Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 50 μA	V <sub>GS(th)</sub>	3.0		4.5	V
Forward Transconductance	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.0 A	g <sub>FS</sub>		3.3		S

### DYNAMIC CHARACTERISTICS

Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	C <sub>iss</sub>		535		pF
Output Capacitance		C <sub>oss</sub>		62		
Reverse Transfer Capacitance		C <sub>rss</sub>		14		
Total Gate Charge	V <sub>DD</sub> = 310 V, I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 10 V	Q <sub>g</sub>		19		nC
Gate-to-Source Charge		Q <sub>gs</sub>		3.9		
Gate-to-Drain ("Miller") Charge		Q <sub>gd</sub>		10		
Plateau Voltage		V <sub>GP</sub>		6.4		V
Gate Resistance		R <sub>g</sub>		4.7		Ω

### RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	V <sub>DD</sub> = 310 V, I <sub>D</sub> = 4.0 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 5 Ω	t <sub>d(on)</sub>		12		ns
Rise Time		t <sub>r</sub>		13		
Turn-Off Delay Time		t <sub>d(off)</sub>		25		
Fall Time		t <sub>f</sub>		14		

### SOURCE-DRAIN DIODE CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Diode Forward Voltage	I <sub>S</sub> = 4.0 A, V <sub>GS</sub> = 0 V	V <sub>SD</sub>			1.6	V
Reverse Recovery Time	V <sub>GS</sub> = 0 V, V <sub>DD</sub> = 30 V, I <sub>S</sub> = 4.0 A, di/dt = 100 A/μs	t <sub>rr</sub>		285		ns
Reverse Recovery Charge		Q <sub>rr</sub>		1.3		μC

4. Insertion mounted

5. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

# NDF04N62Z, NDD04N62Z

## TYPICAL CHARACTERISTICS

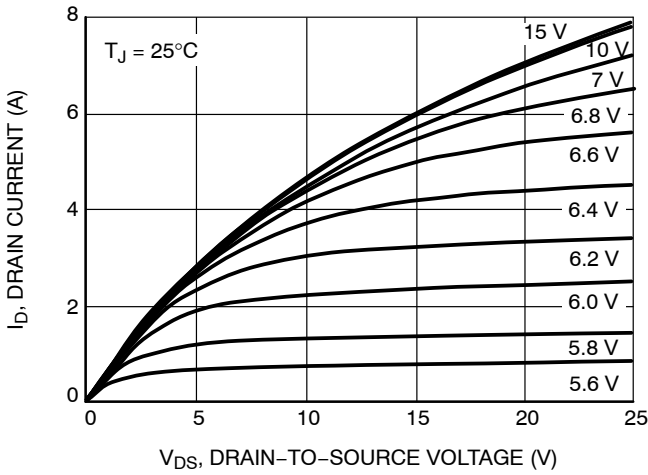


Figure 1. On-Region Characteristics

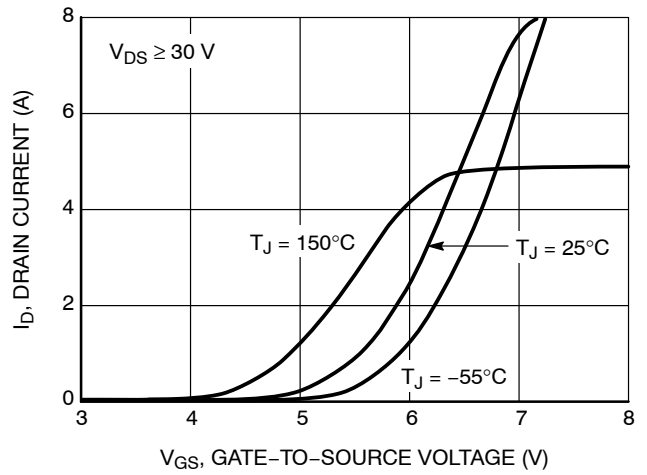


Figure 2. Transfer Characteristics

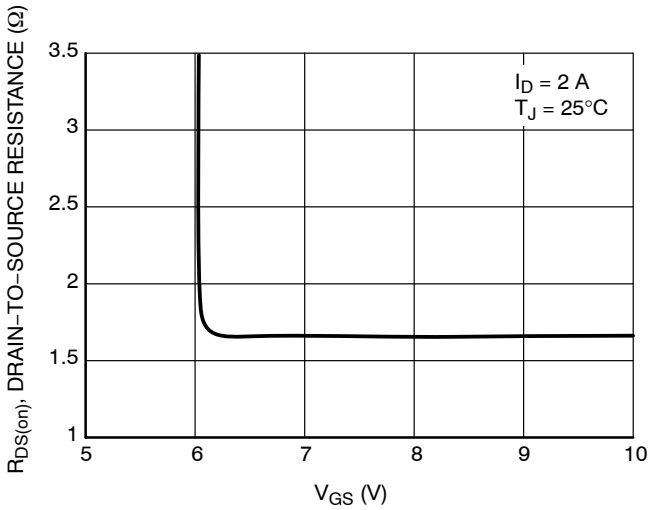


Figure 3. On-Resistance vs. Gate Voltage

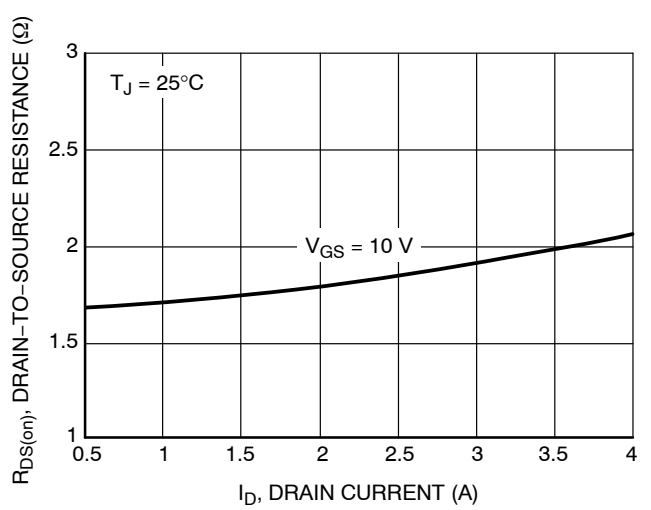


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

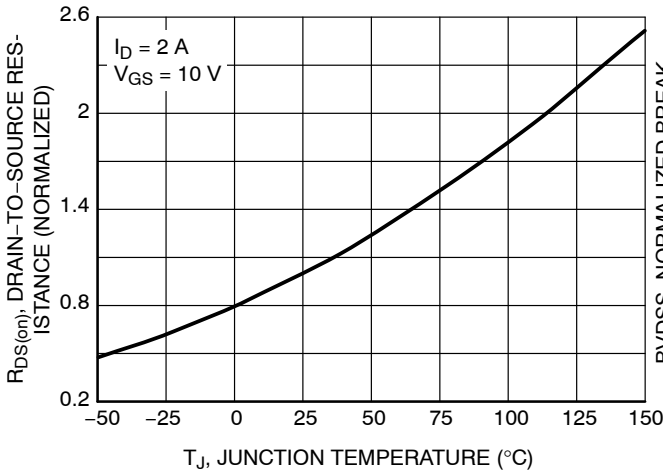


Figure 5. On-Resistance Variation with Temperature

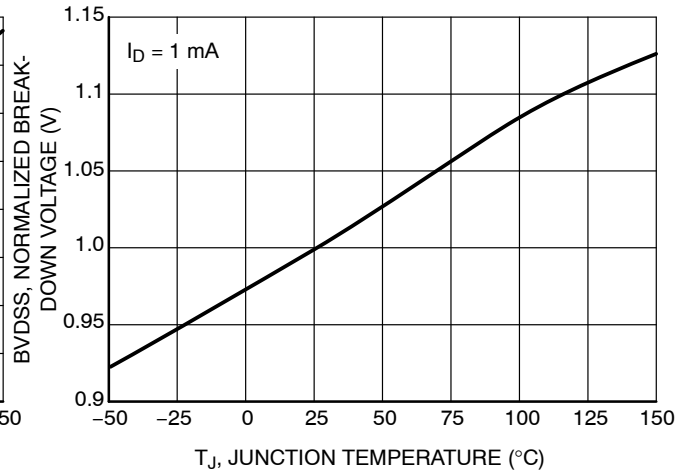
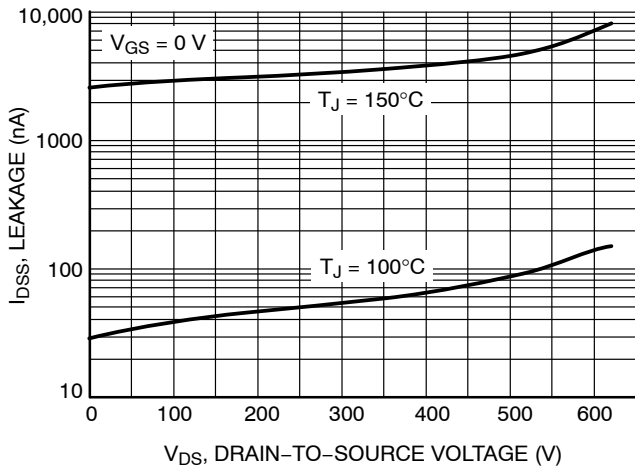


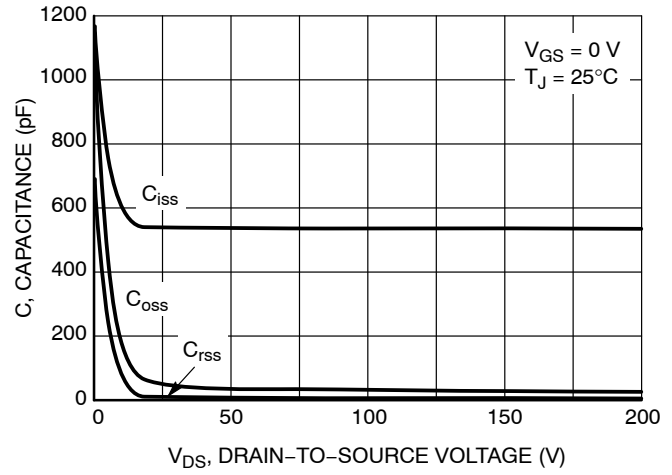
Figure 6. BVDSS Variation with Temperature

# NDF04N62Z, NDD04N62Z

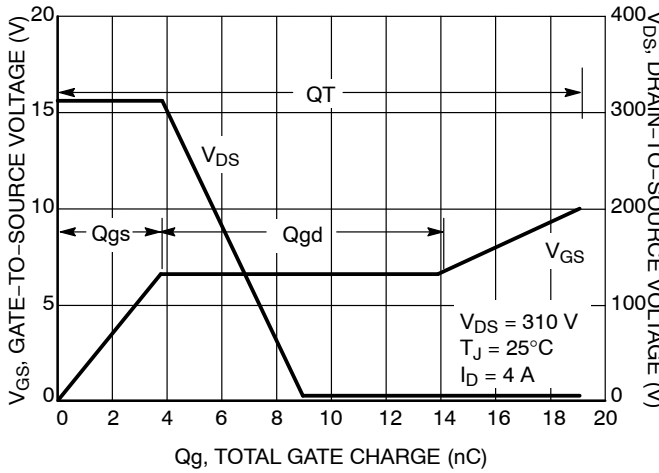
## TYPICAL CHARACTERISTICS



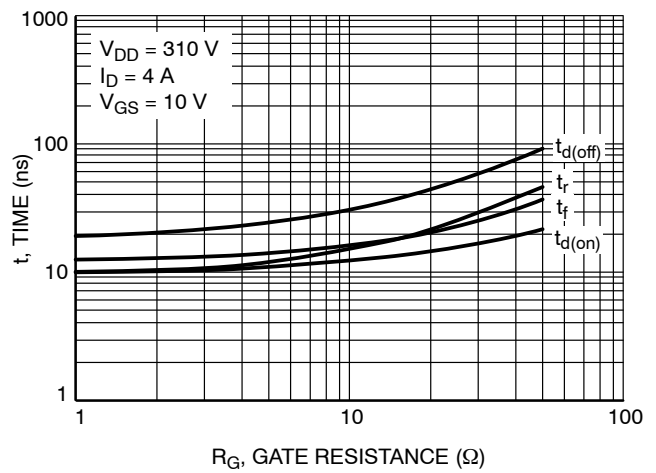
**Figure 7. Drain-to-Source Leakage Current vs. Voltage**



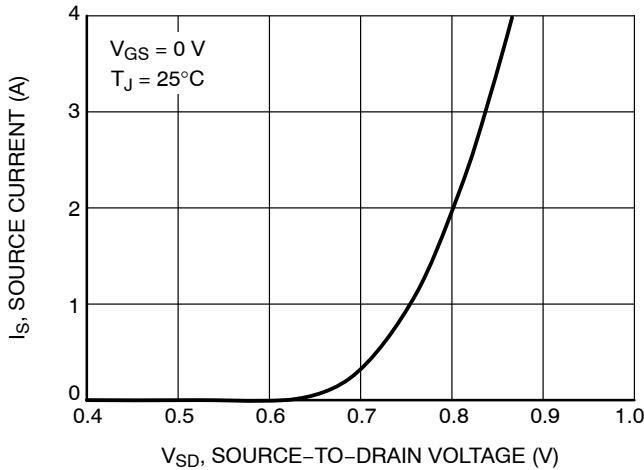
**Figure 8. Capacitance Variation**



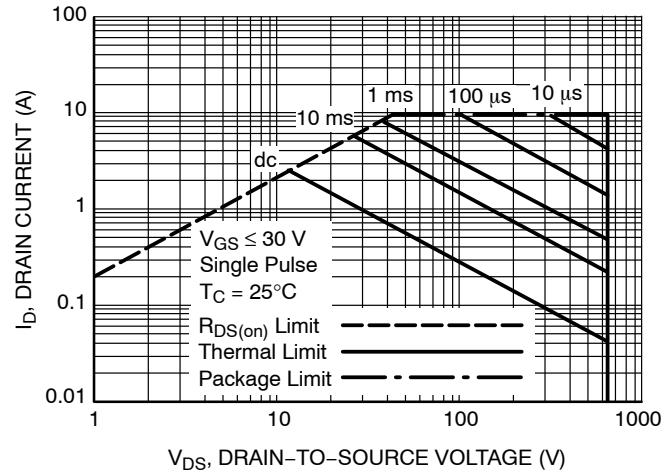
**Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge**



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 11. Diode Forward Voltage vs. Current**



**Figure 12. Maximum Rated Forward Biased Safe Operating Area for NDF04N62Z**

# NDF04N62Z, NDD04N62Z

## TYPICAL CHARACTERISTICS

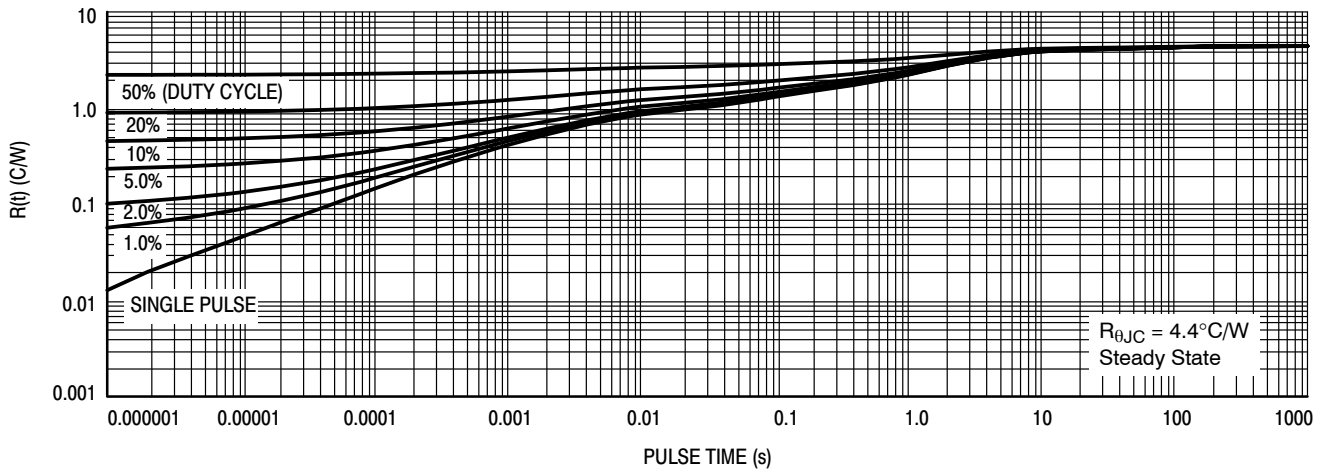


Figure 13. Thermal Impedance for NDF04N62Z

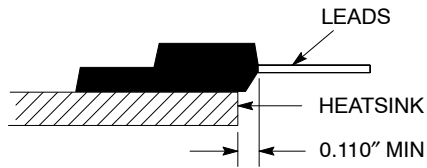


Figure 14. Isolation Test Diagram

Measurement made between leads and heatsink with all leads shorted together.

\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

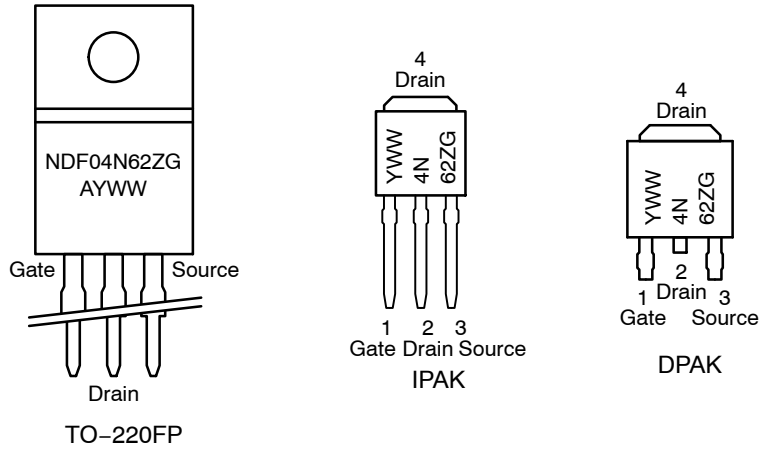
# NDF04N62Z, NDD04N62Z

## ORDERING INFORMATION

Order Number	Package	Shipping†
NDF04N62ZG	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDD04N62Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail (In Development)
NDD04N62ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel (In Development)

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS

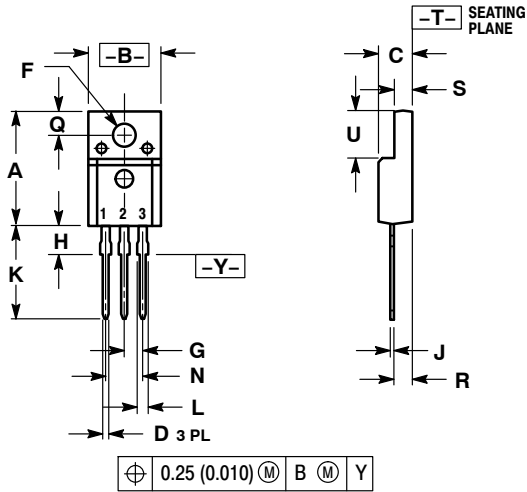


A = Location Code  
 Y = Year  
 WW = Work Week  
 G = Pb-Free, Halogen-Free Package

# NDF04N62Z, NDD04N62Z

## PACKAGE DIMENSIONS

### TO-220FP CASE 221D-03 ISSUE K

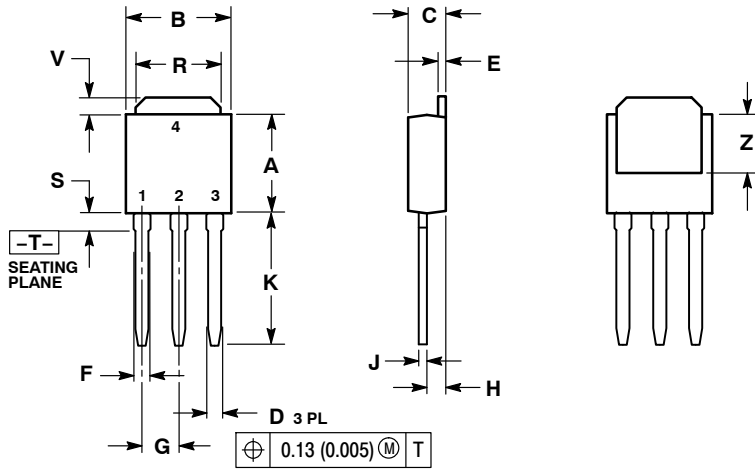


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH
  3. 221D-01 THRU 221D-02 OBSOLETE, NEW STANDARD 221D-03.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

- STYLE 1:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE

### IPAK CASE 369D-01 ISSUE C



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

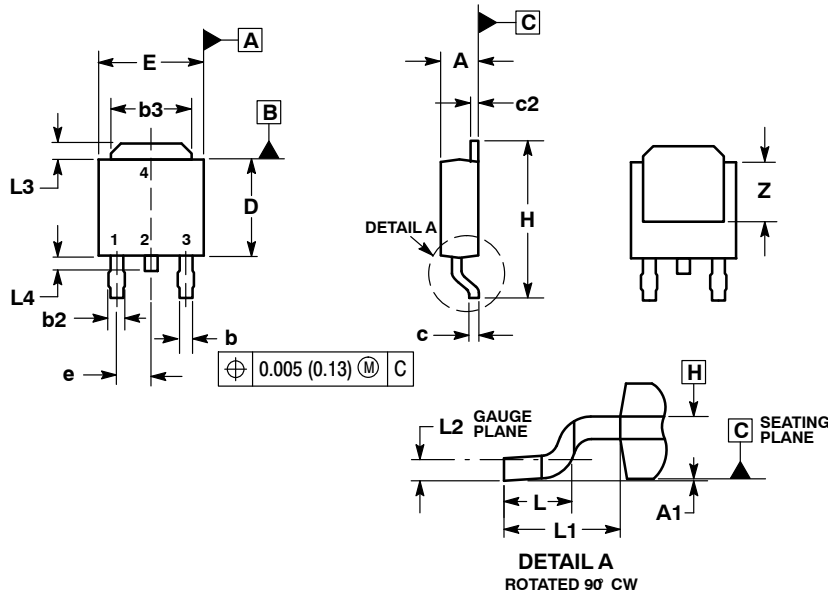
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	----	3.93	----

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

# NDF04N62Z, NDD04N62Z

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369AA-01 ISSUE B



**NOTES:**

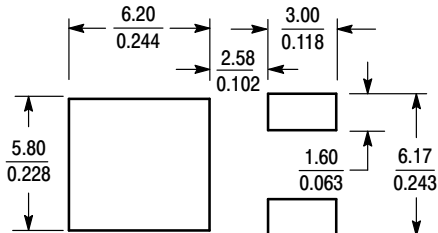
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

**STYLE 2:**

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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